Mikhael Lerman

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SKILLS AND ACCOMPLISHMENTS

- SYSTEM ARCHITECTURE and solutions: RISC-V | x86 PC | ARM | Xilinx Zynq | micro-controller 8051 | Memory DRAM, DDR4, SPI, NVMe, NAND SSD, Micro-SD, NOR SPI, JTAG
- HARD/SOFT Engineering: Firmware and drivers | Web User Interface | Linux kernel and drivers | UEFI x64 Shell | BASH | Batch | PHP | Python | C/C++ | C# | Windows | Linux | SVN | GIT | Graphing with D2
- Network Web and Security: Secure boot | ACRTM | HTML, CSS, Javascript | Backend server side native CGI, PHP, Node.js | Database MySQL | WAMP, LAMP
- Bring up and validation : Logic Analyser | scope | Protocol analysers SATA/SAS, USB, and PCIe | JTAG | Test automation
- Invented Netmory, US patent 9697114 : A new computer architecture for a non volatile and unlimited system memory.
- Invented the BMC : Board Management Controller. SLEEP PROCESSOR: US patent 8683247.
- Other patents include : AUTO-SLEEP ARRAY: US patent 8370669, and EASY FLASH: US patent 9870220.
- AMD Spotlight Award for the outstanding contribution to the Bring up effort with the development of Register Explorer.
- Yocto project (Microchip), Peta-Linux (Xilinx), embedded Linux (Micron)

WORK EXPERIENCE

Firmware Engineer – Datacenter security | MICROSOFT, Mountain View CA 11/2023 to 8/2024

Developed firmware code for the RISC-V security processor in relation to the super computer project. Developed a CLI (Command Line Interface) debug console for the said processor. GIT, VS-Code, RISC-V E20 (Si-Five) tool chain.

Principal Engineer - University Relation and Training | MICROCHIP, San Jose CA 03/2021 to 11/2023

Managed the university program * Created the FPGA RISC-V low cost university kit. * engaged with 28 universities around the world. * Conducted training and support for faculty staff members and students. * Advocated the adoption of the RISC-V in the curriculum of the universities. * Developed training material about computing with RISC-V, bare metal applications. * Created a wide network with the academia.

Customer Firmware Engineer NVMe Products | SAMSUNG, San Jose CA 10/2018 to 02/2021

SSD drive Firmware. Formal code releases of the NVMe Samsung drives. Resolve firmware issues. Lauterbach Trace32 JTAG debugger. Automation involving SVN, JIRA, Confluence, Jenkins and Linux target. Development of new customer features through VUC (Vendor Unique Command).

Staff Debug/Diagnostic Engineer | Xilinx, San Jose CA 08/2017 to 08/2018

Design and verification of DFx features with Vivado and Synopsys DVE on DSP device. Firmware test of DRAM memory and

L2 cache running out of On Chip Memory.

Firmware development Engineer | Comcast Innovation Center, San Jose CA 06/2017 to 08/2017

RDK-B, Yocto, Linux, development of security features for the Comcast wireless gateways.

Software Engineer - Senior | Micron, Milpitas CA 03/2014 to 06/2017

Embedded Business Unit. SPI Secure boot. Cryptographic hash mac, SHA256, key generation. Linux Kernel : SPI protocol driver, FSBL UBOOT. Android with Snapdragon, ADB. BSP from Intrinsyc Open-Q 820.

Senior Staff Engineer | INPHI, San Jose CA 01/2013 to 03/2014

Firmware BIOS: Intel Memory Reference Code with AMI BIOS. DDR4, UEFI, system memory, NVDIMM.

System Engineering Manager | AMD, Sunnyvale CA 05/2000 to 01/2013

AMD core logic and chipset. JTAG Dfx, Embedded Board Management Controller.

System Solution Manager | STMICROELECTRONICS, Saint-Genis Pouilly France 11/1994 to 05/2000

Managed a multi-disciplinary team. Key contribution to the emergence of the first x86 SoC of the industry : the STPC.

Hardware Design Engineer | Normerel, Buc France 11/1990 to 11/1994

Designed few of the first IBM PC compatible micro-computers.

E D U C A T I O N

BSC Bachelor of Science | Technion - Israel Institute of Technology, Haifa, Israel Graduation 1990

L A N G U A G E S

French | English | Hebrew | Arabic